

Claims

What is claimed is:

1. An image capture system comprising,
a pixel comprising:

5 a first FET having a gate terminal coupled to a
reset line for providing a reset signal, a drain
terminal coupled to a supply voltage, and a source
terminal; and

10 a photodetector coupled between a first ground and
the source terminal of the first FET;

 a first switching device selectively coupled to the
reset line; and

 a reference voltage source coupled between a second
ground and the reset line via the first switching device,

15 wherein the reference voltage source generates a ground
referenced reset voltage and the first and second grounds
have the same potential.

2. The image capture system of claim 1, further comprising
20 an operational amplifier buffer coupled between the reset
line and the reference voltage source.

3. The image capture system of claim 1, wherein the first
FET further comprises an n-channel enhancement mode MOSFET.

4. The image capture system of claim 1, wherein the ground referenced reset voltage is greater than the supply voltage.

5 5. The image capture system of claim 1, further comprising a second FET having a gate terminal coupled to the source terminal of the first FET and a drain terminal coupled to the supply voltage.

10 6. The image capture system of claim 5, further comprising a third FET having a gate terminal coupled to a row select line, a source terminal coupled to a column line, and a drain terminal coupled to a drain terminal of the second FET.

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7. An apparatus comprising:

a pixel having a photodetector coupled to a reset transistor, the reset transistor being configured to receive a reset signal;

20 a reference voltage source coupled to the reset transistor for providing the reset signal to the reset transistor; and

a supply voltage source coupled to the reset transistor for resetting the photodetector between exposure intervals.

8. The apparatus of claim 7, wherein the photodetector and the reference voltage source are each grounded to a common potential.

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9. The apparatus of claim 7, wherein the photodetector is grounded at a ground voltage and the reset signal is equal to the reference voltage or the reference voltage plus a boost level when the reset signal is asserted high and is equal to the ground voltage when asserted low.

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10. The apparatus of claim 7, wherein the reset transistor comprises an n-channel enhancement mode MOSFET.

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11. The apparatus of claim 7, wherein the reset transistor comprises an n-channel enhancement mode MOSFET having a gate terminal coupled to the reference voltage source, a drain terminal coupled to the supply voltage, and a source terminal coupled to the photodetector.

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12. The apparatus of claim 7, wherein the photodetector comprises a photodiode.

13. The apparatus of claim 7, further comprising a switching device coupled between the reference voltage source and the reset transistor.

5 14. The apparatus of claim 13, wherein the switching device comprises a multiplexer.

15. A method comprising:

providing a first reset signal to a pixel, the first
10 reset signal being equal to a reference voltage;

resetting the pixel in response to the first reset signal using a supply voltage, the supply voltage being different from the reference voltage;

reading a first voltage value generated at the pixel
15 following a light exposure interval;

providing a second reset signal to the pixel, the second reset signal being equal to the reference voltage;

reading a second voltage value from the pixel; and

generating a pixel value using the first and the second
20 voltage values.

16. The method of claim 15, wherein the pixel value equals the second voltage value minus the first voltage value.

17. The method of claim 15, wherein the first voltage value is approximately proportional to a light intensity detected by the pixel during the light exposure interval.

5 18. The method of claim 15, further comprising repeating the providing a first reset signal to a pixel, reading a first voltage value, providing a second reset signal to the pixel, reading, and generating for a plurality of pixels.

10 19. The method of claim 15, wherein the generating is performed by a column circuit.

20. The method of claim 15 wherein the reading a first voltage value comprises exposing a photodiode to incident
15 light.